

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|-------------------------|--|------------------|
| 1 | BRS | L1 | 3 | kim near seong-wook.in. | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/08 11:09 |
| 2 | BRS | L2 | 677 | 438/199.ccls. | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/08 11:10 |
| 3 | BRS | L3 | 8 | 2 and (ddd) | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/08 11:17 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|-------|--------------------------------|--|----------------------|
| 4 | BRS | L4 | 6 | 2 and (double-diffused) | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/0 8 11:21 |
| 5 | BRS | L5 | 13 | 2 and (double-diffused or ddd) | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/0 8 11:25 |
| 6 | BRS | L6 | 11924 | (double-diffused or ddd) | US-PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/0 8 11:26 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|------|-----|------|--|--|----------------------|
| 7 | BRS | L7 | 85 | (double-diffused or ddd) near15 ((spacer\$1 or sidewall\$1) or (side near wall\$1)) | US- PGPUB ; USPAT ; EPO; JPO; DERWE NT; IBM_T DB | 2004/12/0 8 11:48 |

| | U | 1 | Document ID | Title | Current OR |
|---|---|---|-------------------------|---|------------|
| 1 | | | US 20020123182 A1 | TRANSISTOR WITH ULTA-SHORT GATE FEATURE AND METHOD OF FABRICATING THE SAME | 438/199 |
| 2 | | | US 20020102780 A1 | Semiconductor device and manufacturing method thereof | 438/199 |
| 3 | | | US 20020048914 A1 | METHOD OF FABRICATING A SEMICONDUCTOR DEVICE OF HIGH-VOLTAGE CMOS STRUCTRE | 438/549 |
| 4 | | | US 6806134 B2 | Sidewall strap for complementary semiconductor structures and method of making same | 438/233 |

| | U | 1 | Document ID | Title | Current OR |
|---|---|---|------------------|---|------------|
| 5 | | | US 6746906 B2 | Transistor with ultra-short gate feature and method of fabricating the same | 438/199 |
| 6 | | | US 6512273 B1 | Method and structure for improving hot carrier immunity for devices with very shallow junctions | 257/369 |
| 7 | | | US 6391698 B1 | Forming complementary metal-oxide semiconductor with gradient doped source/drain | 438/199 |
| 8 | | | US 6255152 B1 | Method of fabricating CMOS using Si-B layer to form source/drain extension junction | 438/199 |

| | U | 1 | Document ID | Title | Current OR |
|----|---|---|---------------|---|------------|
| 9 | | | US 6187620 B1 | Integrated circuit having sacrificial spacers for producing graded NMOS source/drain junctions possibly dissimilar from PMOS source/drain junctions | 438/230 |
| 10 | | | US 6069031 A | Process to form CMOS devices with higher ESD and hot carrier immunity | 438/197 |
| 11 | | | US 5837572 A | CMOS integrated circuit formed by using removable spacers to produce asymmetrical NMOS junctions before asymmetrical PMOS junctions for optimizing thermal diffusivity of dopants implanted therein | 438/199 |

| | U | 1 | Document ID | Title | Current OR |
|----|---|---|--------------|--|------------|
| 12 | | | US 5702988 A | Blending integrated circuit technology | 438/238 |
| 13 | | | US 4318750 A | Method for radiation hardening semiconductor devices and integrated circuits to latch-up effects | 438/798 |